UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/631,205	07/31/2003	Gerard Chauvel	TI-35432 (1962-05411)	3321

23494 7590 11/02/2006

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
RUTZ, JARED IAN	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 11/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/631,205	CHAUVEL ET AL.	
	Examiner	Art Unit	
	Jared I. Rutz	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-18 as amended on 8/25/2006 are pending in the instant application. Applicant's arguments regarding the rejection of claims 1, 2, 9, and 10 under 35 USC 102(e), see the paragraph spanning pages 7 and 8 have been carefully and fully considered by the examiner, and are persuasive. This Office action contains a new grounds of rejection not necessitated by amendment, and is accordingly is non-final.

Specification

2. The amendment to the specification submitted 8/25/2006 is accepted by the Examiner.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 1-3, 6, 9-11, 14, and 17-18** are rejected under 35 U.S.C. 102(b) as being anticipated by Adams, III et al. (US 6,151,661).

5. **Claim 1** is taught by Adams as:

a. *A method of managing memory, comprising: issuing a data request to remove data*. Column 4 lines 55-56 show that a POP operation is issued by processor 12.

b. *Determining whether the data is being removed from a cache line in a cache memory*. Figure 3 shows that different processing for a POP operation is performed depending on whether or not the data being popped is in the cache.

c. *Determining whether the data being removed is stack data*. Column 4 lines 34-38 shows that a signal is provided to indicate if the read operation is a POP operation or a normal read.

d. *And varying the memory management policies depending on whether the data being removed corresponds to a predetermined word in the cache line*. Column 4 line 66 to column 5 line 6 shows that if the popped data word is the highest address word in the cache line, the processor invalidates the cache line. Column 4 lines 61-65 show that if the popped word is not the highest address word, a normal cache operation ensues.

6. **Claim 2** is taught by Adams as:

e. *The method of claim 1, wherein the predetermined word is the first word in the cache line*. Column 4 line 66 to column 5 line 6 shows that if the popped data word is the highest address word in the cache line, the processor invalidates the cache line. As shown in figure 2, in the direction of a push operation the highest address word is first in the cache line.

7. **Claim 3** is taught by Adams as:

f. *The method of claim 2, wherein the cache line is invalidated.* Column 4 line 66 to column 5 line 6 shows that if the popped data word is the highest address word in the cache line, the processor invalidates the cache line.

8. **Claim 6** is taught by Adams as:

g. *The method of claim 1, wherein the predetermined word is the last word in the cache line.* Column 4 line 66 to column 5 line 6 shows that if the popped data word is the highest address word in the cache line, the processor invalidates the cache line. As shown in figure 2, in the direction of a pop operation the highest address word is the last word in the cache line.

9. **Claim 9** is taught by Adams as:

h. *A system, comprising: a memory.* Figure 1 items 14 and 18.

i. *A controller coupled to the memory.* Figure 1 item 16.

j. *A stack that exists in the memory.* Column 3 lines 54- 57 shows that stacks are stored within the cache.

k. *Wherein the memory further comprises a cache memory and a main memory.* Figure 1 item 14 is a cache and item 18 is main memory.

l. *And wherein the controller adjusts its management policies depending on whether data that is being removed corresponds to a predetermined word in a*

cache line. Column 4 line 66 to column 5 line 6 shows that if the popped data word is the highest address word in the cache line, the processor invalidates the cache line. Column 4 lines 61-65 show that if the popped word is not the highest address word, a normal cache operation ensues.

10. **Claim 10** is taught by Adams as:

m. *The system of claim 9, wherein the predetermined word is the first word in the cache line.* Column 4 line 66 to column 5 line 6 shows that if the popped data word is the highest address word in the cache line, the processor invalidates the cache line. As shown in figure 2, in the direction of a push operation the highest address word is first in the cache line.

11. **Claim 11** is taught by Adams as:

n. *The system of claim 10, wherein the cache line is invalidated.* Column 4 line 66 to column 5 line 6 shows that if the popped data word is the highest address word in the cache line, the processor invalidates the cache line.

12. **Claim 14** is taught by Adams as:

o. *The system of claim 9, wherein the predetermined word is the last word in the cache line.* Column 4 line 66 to column 5 line 6 shows that if the popped data word is the highest address word in the cache line, the processor invalidates the

cache line. As shown in figure 2, in the direction of a pop operation the highest address word is the last word in the cache line.

13. **Claim 17** is taught by Adams as:

p. *A system, comprising: a processor that executes stack-based instructions.* Column 1 lines 55-58.

q. *A cache controller coupled to the processor.* Stack cache support logic 16, see column 4 lines 38-42.

r. *A cache memory coupled to and controlled by said cache controller.* Figure 1 item 14.

s. *Said cache memory storing at least a portion of a stack.* Column 3 lines 54- 57 shows that stacks are stored within the cache.

t. *Said stack having a top and a read access of the stack causes the top of the stack to be read.* Column 1 lines 26-32.

u. *Wherein the controller invalidates an entire line of said cache memory upon the processor reading a value from the top of the stack if said value from the top of the stack comprises a word at a predetermined location with said line.* Column 4 line 66 to column 5 line 6 shows that if the popped data word is the highest address word in the cache line, the processor invalidates the cache line.

14. **Claim 18** is taught by Adams as:

v. *The system of claim 17 wherein said predetermined location is selected from a group consisting of the first word and the last word of the line.* As shown in figure 2, in the direction of a push operation the highest address word is first in the cache line.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. **Claims 4-5** are rejected under 35 U.S.C. 103(a) as being unpatentable over Adams (cited supra) in view of Handy (The Cache Memory Book).

17. **Claim 4** is taught by Adams as shown supra with respect to claim 2.

18. Although Adams teaches that a cache line should be invalidated and made available for valid data when a popped word is the highest address word in the cache line (column 5 lines 2-6), Adams does not disclose expressly that the cache line is queued for replacement by a replacement policy.

19. With respect to claim 4 Handy teaches that if the cache is a multi-way cache, an algorithm must be used to select a line to be replaced, page 57 lines 3-14.

20. Handy and Adams are analogous art because they are from the same field of endeavor, the design of caches.

21. At the time of the invention it would have been obvious to use a multi-way set associative cache in the system of Adams.

22. The motivation for doing so would have been to lessen thrashing while still improving the hit rate over a direct mapped cache, Handy page 54 lines 1-18.

23. Therefore it would have been obvious to combine Handy with Adams for the benefit of reducing thrashing while improving hit rate to obtain the invention as specified in **claims 4-5**.

24. **Claim 5** is taught by Handy as:

w. *The method of claim 4, wherein the replacement policy is a least recently used (LRU) policy.* Page 57 lines 10-14 teaches the use of a LRU replacement algorithm.

25. **Claims 7-8** rejected under 35 U.S.C. 103(a) as being unpatentable over Adams (cited supra) in view of Flake (US 7,065,613).

26. **Claim 7** is taught by Adams as shown supra with respect to claim 1.

27. Adams dose not explicitly address the situation in which a cache line is dirty.

28. With respect to claim 7, Flake teaches:

x. *The method of claim 1, wherein the cache line is a dirty cache line.* As shown by Flake in lines 50-63, a cache line can be dirty, and a dirty cache line should be written to memory.

29. Adams and Flake are analogous art because they are both from the same field of endeavor, the design of computer data caches.

30. At the time of the invention, it would have been obvious to one of ordinary skill in the art that a dirty cache line may be removed from a cache.

31. The motivation for doing so would have been to allow changed data stored in the cache to be transferred to main memory, and therefore not lost. Additional motivation comes from Flake at column 4 lines 1-2, which incorporates Adams by reference.

32. Therefore it would have been obvious to one of ordinary skill in the art to combine Flake with Adams for the benefit of not losing updated data in the cache to obtain the invention as specified in **claims 7-8**.

33. **Claim 8** is taught by Adams and Flake as:

y. *The method of claim 7, further comprising, invalidating the dirty cache line if the predetermined word in the dirty cache line is the first word.* Column 4 line 66 to column 5 line 6 shows that if the popped data word is the highest address word in the cache line, the processor invalidates the cache line. As shown in figure 2, in the direction of a push operation the highest address word is first in the cache line. As shown by Flake at lines 50-63, a dirty line can be invalidated, but the data stored therein must be written to main memory when the line is replaced.

34. **Claims 12-13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Adams (cited supra) in view of Handy (cited supra).

35. **Claim 12** is taught by Adams as shown supra with respect to claim 2.

36. Although Adams teaches that a cache line should be invalidated and made available for valid data when a popped word is the highest address word in the cache line (column 5 lines 2-6), Adams does not disclose expressly that the cache line is queued for replacement by a replacement policy.

37. With respect to claim 4 Handy teaches that if the cache is a multi-way cache, an algorithm must be used to select a line to be replaced, page 57 lines 3-14.

38. Handy and Adams are analogous art because they are from the same field of endeavor, the design of caches.

39. At the time of the invention it would have been obvious to use a multi-way set associative cache in the system of Adams.

40. The motivation for doing so would have been to lessen thrashing while still improving the hit rate over a direct mapped cache, Handy page 54 lines 1-18.

41. Therefore it would have been obvious to combine Handy with Adams for the benefit of reducing thrashing while improving hit rate to obtain the invention as specified in **claims 12-13**.

42. **Claim 13** is taught by Handy as:

z. *The system of claim 12, wherein the replacement policy is LRU.* Page 57 lines 10-14 teaches the use of a LRU replacement algorithm.

43. **Claims 15-16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Adams (cited supra) in view of Flake (US 7,065,613).

44. **Claim 15** is taught by Adams as shown supra with respect to claim 9.

45. Adams dose not explicitly address the situation in which a cache line is dirty.

46. With respect to claim 15, Flake teaches:

aa. *The method of claim 9, wherein the cache line is a dirty cache line.* As shown by Flake in lines 50-63, a cache line can be dirty, and a dirty cache line should be written to memory.

47. Adams and Flake are analogous art because they are both from the same field of endeavor, the design of computer data caches.

48. At the time of the invention, it would have been obvious to one of ordinary skill in the art that a dirty cache line may be removed from a cache.

49. The motivation for doing so would have been to allow changed data stored in the cache to be transferred to main memory, and therefore not lost. Additional motivation comes from Flake at column 4 lines 1-2, which incorporates Adams by reference.

50. Therefore it would have been obvious to one of ordinary skill in the art to combine Flake with Adams for the benefit of not losing updated data in the cache to obtain the invention as specified in **claims 15-16**.

51. **Claim 16** is taught by Adams and Flake as:

bb. *The method of claim 15, further comprising, invalidating the dirty cache line if the predetermined word in the dirty cache line is the first word.* Column 4 line 66 to column 5 line 6 shows that if the popped data word is the highest address word in the cache line, the processor invalidates the cache line. As shown in figure 2, in the direction of a push operation the highest address word is first in the cache line. As shown by Flake at lines 50-63, a dirty line can be invalidated, but the data stored therein must be written to main memory when the line is replaced.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jared I. Rutz whose telephone number is (571) 272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jared I Rutz
Examiner
Art Unit 2187

jir

Brian R. Peugh
Primary Examiner